Detection of electromagnetic radiation in Standard CMOS SOI

Grating enhanced detectors in 45nm and 32nm standard CMOS SOI

Matthias Fertig et. al.

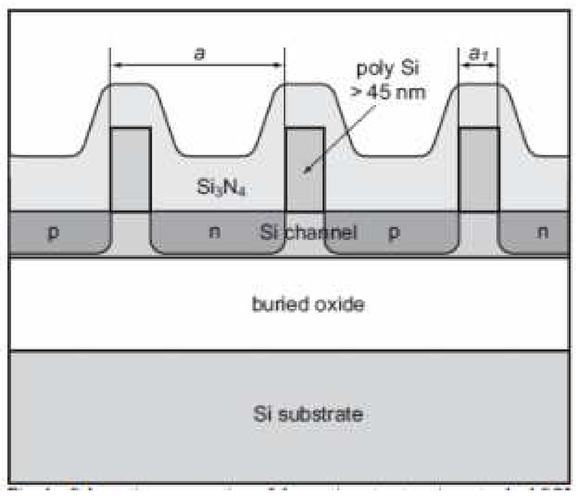
The absorption of electromagnetic radiation is a fundamental challenge in various applications like optical on-chip detectors, usable for chip-to-chip communication. Monolithic solutions are desirable, but the standard technologies significantly limit the design space by design rules and materials.

For optical on-chip detectors, a wide variety of hybrid solutions exist which did not make their way to industrial solutions and mass products yet mainly by cost and reliability reasons. A monolithic design, fully compliant with standard semiconductor technology, is preferred but requires advanced techniques to significantly enhance the local absorption of light in very thin silicon layers, i.e. in the range of tens of nanometers.

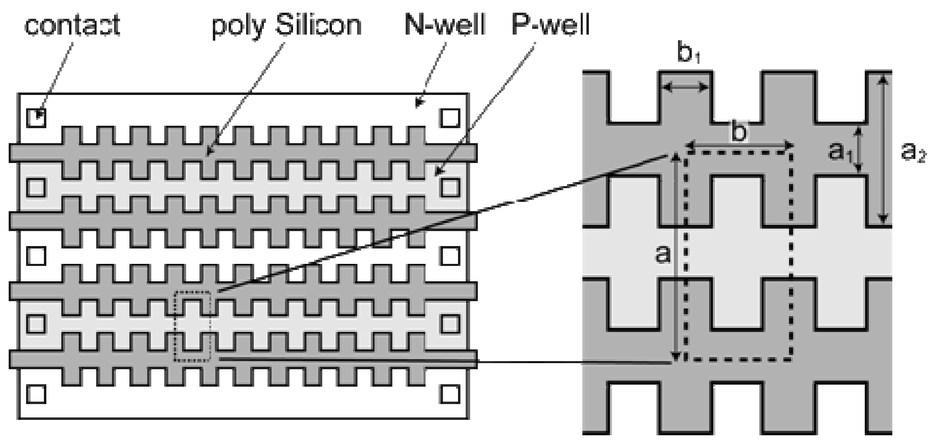
The use of sub-wavelength diffraction gratings show promising results to maximise the local absorption. Here, two on-chip chip optical detectors are implemented in standard CMOS SOI technologies without modifications in the process.

In a first implementation in 45nm standard CMOS SOI, a two-dimensional sub-wavelength diffraction grating is formed from by Poly-Silicon adjacent to the absorbing layer. In a second implementation, an inline grating is used to maximize the local absorption from resonances in the electromagnetic field. There, the grating is formed from Silicon-Dioxide in the same layer as the absorbing layer.

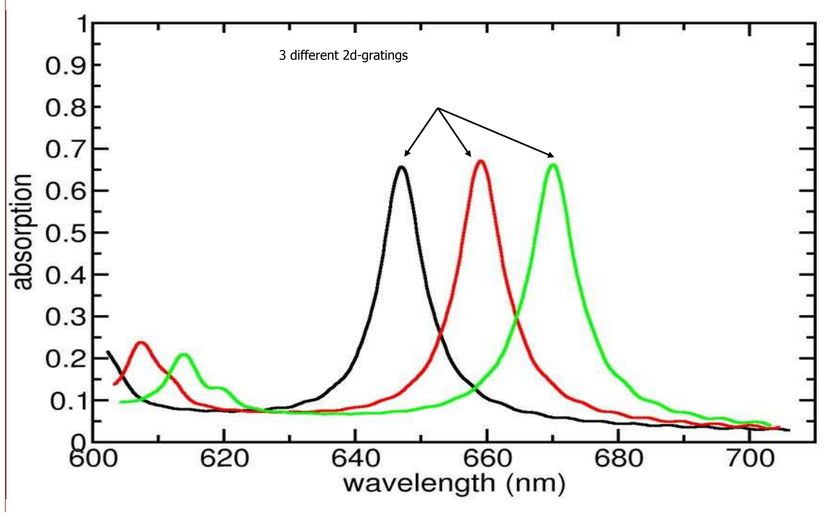
Given: Configuration of layers in a standard CMOS SOI technology



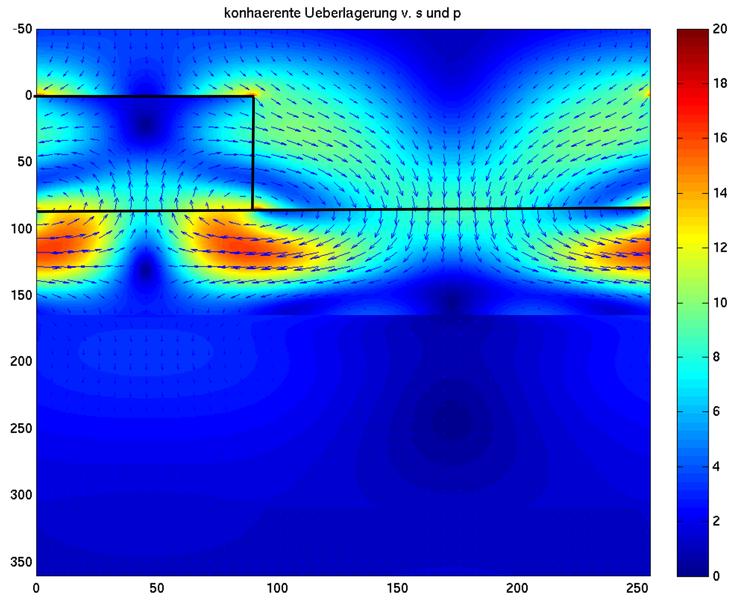
Wanted: A geometry and set of parameters to maximize the local absorption in the active region of a detector, i.e. the Si channel



Absorption for three selected gratings:



Simulation of the Intensity distribution and Poynting Vector for a design in 45nm Standard CMOS SOI



$$\mathbf{S} = \mathbf{E} \times \mathbf{H} = \frac{1}{\mu}\mathbf{E} \times \mathbf{B},$$

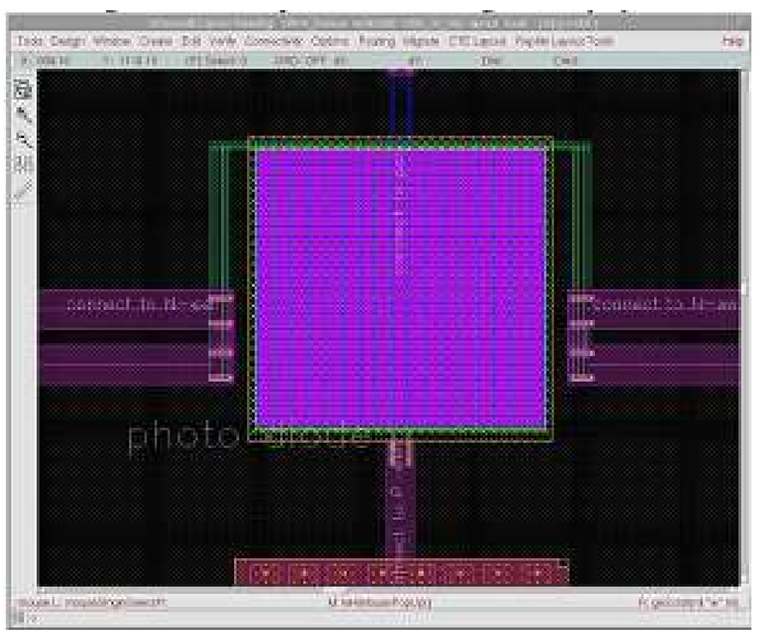
Absorption in a layer of 40nm thickness:

No grating: 8%

1D grating: 25%

2D grating: 66%

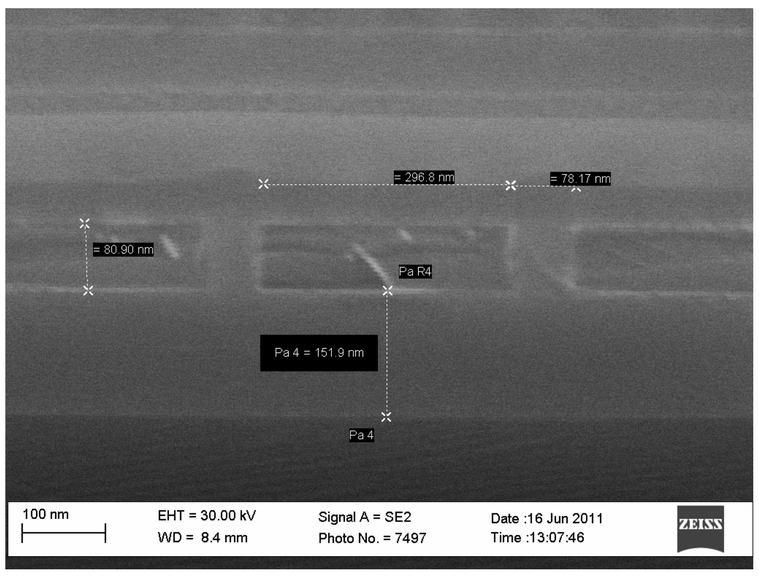
Design in 45nm Standard CMOS SOI



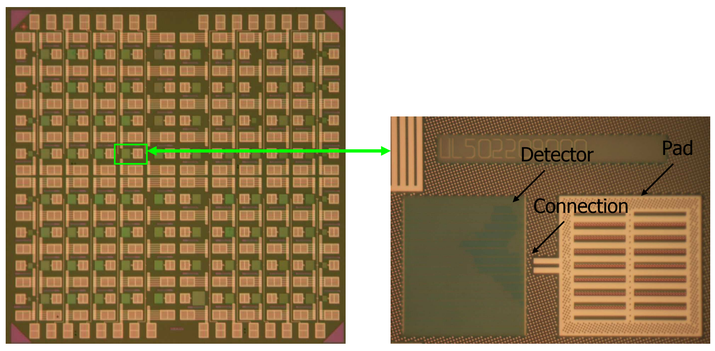
Detector layout:

- fully automated with Cadence SKILL script
- DRC clean design
- sizes from 25x25 up to 100x100 um^2

Photograph of an inline grating in 32nm CMOS SOI taken with a Scanning Electron Microscope



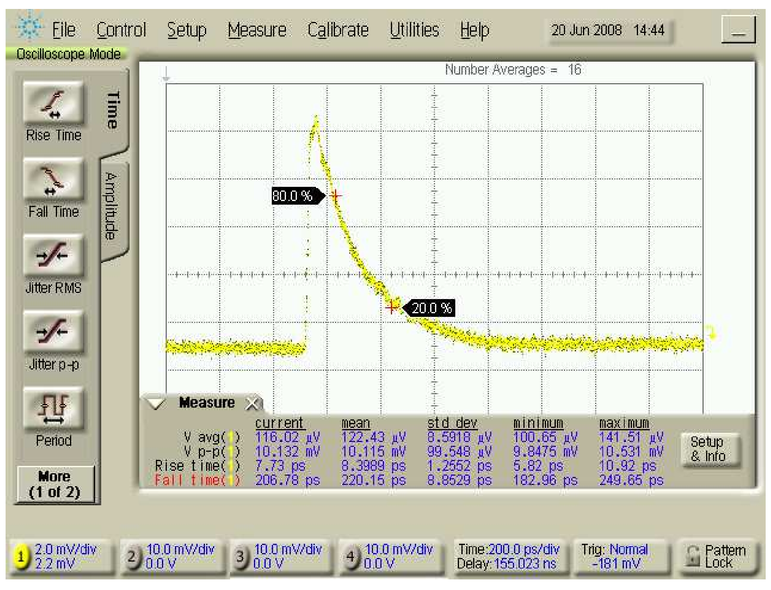
Photograph of the experiment and a detector in 45nm CMOS SOI from a microscope



Detector photograph:

- 80 detectors connected to std pads (left)
- 50x50 um^2 detector (right)

Impulse response obtained from a femto-second pulse



Conclusions: Diffraction gratings are suitable to enhance the local absorption in ultra-thin layers, where the absorption coefficient is not sufficient to harvest significant electromagnetic energy. The presented solutions show a high sensitivity to variations in the geometry and the angle of incidence. The technology and the design rules need a deep analysis to secure device performance and compliance with the technology.

[1] Morf, Fertig, Moll, Pflueger, " Title", Journal of the optical society A, (2008)
[2] Morf, .. IBM Journal of Research (2008)

Prof. Dr. Matthias Fertig
matthias.fertig@htwg-konstanz.de

Braunegger Straße 55
78462 Konstanz

Dr. Thomas Morf
tmr@zrl.ibm.com

Säumerstraße 1
CH-Rüschlikon

Prof. Dr. Karl-Heinz Brenner
brenner@ziti.uni-heidelberg.de

B6,26 3rd floor
68167 Mannheim