RZ 3735 (# 99745) 05/18/2009
Electrical Engineering 5 pages

Research Report

Polarization-Independent Photo-Detectors with Enhanced Responsivity in a Standard SOI CMOS Process

N. Moll[1], T. Morf[1], M. Fertig[2], T. Stöferle[1], B. Trauter[3], R. F. Mahrt[1], J. Weiss[1], T. Pflüger[2], and K.-H. Brenner[3]

[1]IBM Research GmbH
Zurich Research Laboratory
8803 Rüschlikon
Switzerland

[2]IBM Research & Development Böblingen,
Schönaicher Straße 220,
71032 Böblingen,
Germany

[3]Institute for Computer
Engineering of the University of Heidelberg,
68131 Mannheim,
Germany

Polarization-Independent Photo-Detectors with Enhanced Responsivity in a Standard SOI CMOS Process

N. Moll, T. Morf, M. Fertig, T. Stöferle, B. Trauter, R. F. Mahrt, J. Weiss, T. Pflüger, and K.-H. Brenner

Abstract— A polarization-independent photo-detector device is demonstrated that can be combined with electronic integrated circuits on a single chip. The photo-detector device is fully compatible with the standard silicon-on-insulator (SOI) CMOS (complementary metal-oxide-semiconductor) process without requiring process modification or post-processing.

***Index Terms*—Silicon on insulator technology, Photo-detectors, CMOS integrated circuits.**

I. Introduction

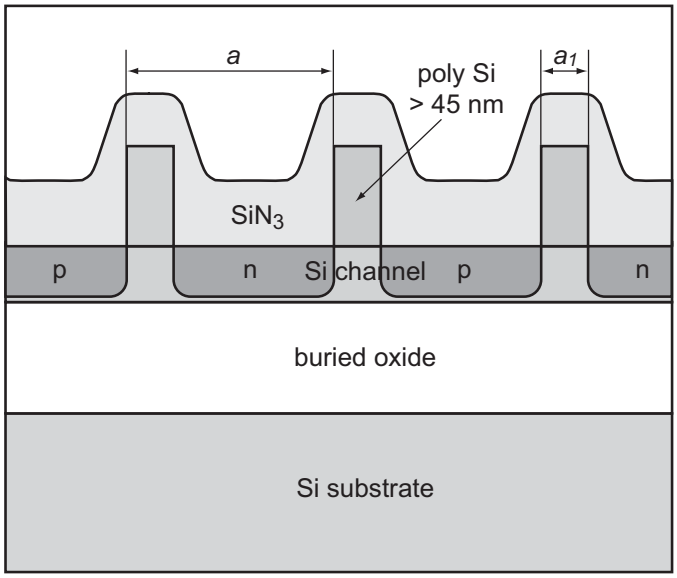
Today the realization of optical chip-to-chip communication is restricted by the challenges of combining optical detectors and light sources with integrated CMOS circuits. Several approaches of how to integrate optical detectors into a commercial CMOS process are described in the literature [1,2]. They range from on-chip photo-diodes (PD) implemented with *pn*-junctions available in the process [1,3] over deep trench memory cells [4] used as detectors to hybrid implementations in which additional semiconductor layers e.g. germanium are placed on top of the chip [5]. Efficient III-V photo-detectors have been attached, on CMOS dies using hybrid approaches [6] or III-V layers have been grown on top of silicon. The latter method is challenging because of the lattice mismatch between Si and III-V semiconductors.

The bandgap of 1.1 eV of silicon satisfies an important prerequisite for short-wavelength detectors. In addition CMOS, or even better BiCMOS (Bipolar CMOS), technologies offer an entire range of *pn*-junctions that can be used to build detectors. However, in state-of-the-art technologies the doping levels are very high. As a result, the depletion regions of such *pn*-junctions are very narrow, approximately 50 to 100 nm. This leads to very high junction capacitances, which severely limit the frequency response of such a detector. The small depletion region will also result in a very small responsivity because of the limited volume available to absorb photons and generate charge carriers.

In this paper we present the implementation of an optical detector in an SOI CMOS process, which presents an even greater challenge than using a bulk technology. In SOI CMOS, the bulk silicon serves only as a mechanical carrier and has no electrical function. Lateral *pn*-junction can easily be fabricated in the active layer. The approximately 70 to 100 nm thick active Si layer is too thin to efficiently absorb light. For a wavelength of 650 nm, the penetration depth in Si is 3 μm, thus only 6% of the light will be absorbed.

Figure 1 depicts a simplified cross section of the front-end-of-line of an SOI technology. The active Si layer, together with the underlying buried oxide and the transition metal oxide on top, can be considered as an absorbing optical waveguide. To increase the absorption of the light, we increase the effective waveguide length by introducing a resonant scattering structure. In our case this structure consists of a second-order grating constructed out of the poly-Si gates, which provide the required feedback.

This paper is organized as follows. In Sec. II we present the functionality of the CMOS-compatible photo-detector and compute its parameters. Next we describe the fabrication of the photo-detector devices and the measurement of their responsivity and transients in Sec. III. Finally in Sec. IV we give a short summary and conclusion.



Manuscript received Mai 4, 2009.

N. Moll, T. Morf ,T. Stöferle, J. Weiss, and R. F. Mahrt are with the IBM Research, Zurich Research Laboratory, Säumerstrasse 4, 8803 Rüschlikon, Switzerland. (e-mail: nim@zurich.ibm.com; tmr@zurich.ibm.com, tof@zurich.ibm.com; rfm@zurich.ibm.com; jwe@zurich.ibm.com;).

M. Fertig and T. Pflüger are with IBM Research & Development Böblingen, Schönaicher Straße 220, 71032 Böblingen, Germany (email: matthias.fertig@de.ibm.com; thomas.pflueger@de.ibm.com).

B. Trauter and K.-H. Brenner are with the Institute for Computer Engineering of the University of Heidelberg, 68131 Mannheim, Germany (email: brenner@ziti.uni-heidelberg.de). B. Trauter's current address is Carl Zeiss SMT AG, Oberkochen, Germany (email: b.trauter@smt.zeiss.com).

II. Design and Simulations

The simplest way to integrate a grating structure for our photo-detector device into a CMOS circuit is to utilize the poly-Si gates as a grating. The poly-Si gates have the appropriate location over a potentially depleted *pn*-region and provide high design flexibility. In Fig. 1, the cross section of such a device is shown. In SOI CMOS for an *n*FET (Negative Channel Field Effect Transistor), the active Si channel is lightly *p*-doped (approximately 10^7) and the source and drain implants on both sides of the gate are heavily *n*-doped. For a *p*FET (Positive Channel Field Effect Transistor) the polarities are reversed. The *p*-doping of the Si channel of our photo-detector is approximately 10^7. On one side of the gate we apply 10^{19} *n*+ doping and on the other side 10^{19} *p*+ doping. This is basically a source-drain implant but with a switched polarity on one side. The result is a lateral *p*-*i*-*n* diode, where the depletion region forms under the poly gate. Furthermore, the gates are repeated with a grating period *a* and form a linear second-order grating. Therefore, the gates are spaced very closely, such that each gate shares a doped region with the neighboring gate. The grating period *a* has to be selected such that the structure forms a second-order grating with a certain resonance wavelength. In this paper we restrict ourselves to a single wavelength, namely, 650 nm. This wavelength is widely used for data transmission through polymer-based waveguides and fibers. However, the proposed photo-detector design will also work for other wavelengths at which Si has a higher absorption. The gratings could also be placed on top of ultra-thin III-V materials.

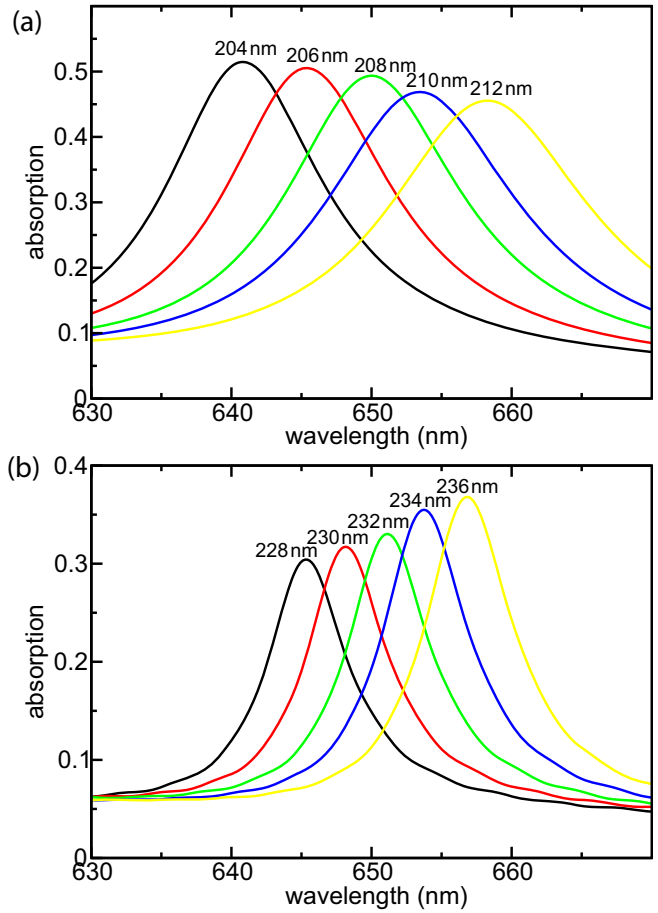


Fig. 2. The absorption of the incident light in the 1D grating as a function of the wavelength for different grating periods *a* for (a) s-polarization and (b) p-polarization. The poly-Si gate width a_1 is kept fixed at 110 nm.

The photo-detector device works as follows. The incident light couples to the second-order grating and forms a standing wave in the device [7]. The standing wave is then absorbed by generating electron-hole pairs. When the electron-hole pairs are generated in the depletion region under the gate and an electric bias voltage is applied, an electric current is created between the *n*- and the *p*-well. Although not every absorbed photon leads to a current, the maximum of the current will coincide with the maximum of the absorption and hence will maximize the absorption.

In the next step, we compute the absorption and grating period *a*. We perform 2D FDTD (Finite-Difference Time-Domain) simulations that calculate the temporal behavior and therefore the actual propagation of the electromagnetic waves in the structure [8]. To obtain the absorption spectra, a calculation cell of size $1a \times 7a$ was used with periodic boundary conditions in the grating direction. The lattice constant *a* is discretized by 20 mesh points. The absorption of Si is implemented by employing material dispersion of the form of one harmonic resonance in the plasmon pole model. The resulting refractive index of Si is 3.78 at a wavelength of 650 nm. For SiO_2, we use a refractive index of 1.45 and for SiN_3 one of 2.02. The grating structure is excited with a perpendicular plane-wave exhibiting a temporal Gaussian envelope and a broad spectral width. The absorption spectrum for both the s- and p-polarization are calculated separately.

For both polarizations the absorption spectra are shown in Fig. 2. The grating period *a* is varied, while keeping the gate width *a1* fixed at 110 nm. For s-polarization, a grating period of 208 nm is necessary to tune the resonance wavelength to 650 nm. The maximum absorption is approximately 0.49. For the p-polarization, a larger grating period of 231 nm is necessary and the maximum absorption decreases to 0.32. Because of the difference in the grating periods, no configuration can be found that absorbs both the s- and the p-polarization equally well at the same time. Even by varying the grating period and the gate length a_1, no such configuration can be found. Consequently, the absorption for polarized light would only be 0.49 or 0.32. However, in most applications unpolarized light would have to be

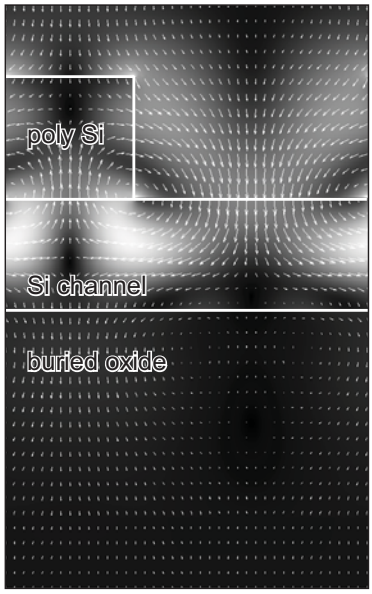


Fig. 3. Contour plot of the intensity and the Poynting vector in the grating structure.

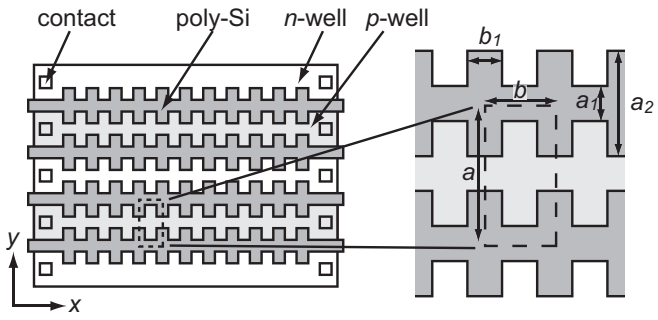


Fig. 4. Top view of the 2D grating structure. The poly-Si gates are defined by its period a in x-direction, its width a_1, its corrugation period b in y-direction, its corrugation width a_2, and its corrugation length b_1.

detected. For unpolarized light the absorption is reduced by a factor two, resulting in 0.24 and 0.16 because half of the light would not couple to the grating.

In Fig. 3 a contour plot of the intensity and the Poynting vector in the grating structure is shown. Approximately half of the light is concentrated below the poly-Si gate in the depletion region of the Si channel. In this region, the absorbed light generates electron-hole pairs that contribute to the signal. However, about half of the light is also absorbed in regions where it does not contribute to the signal. With only half the light coupled to the active area of which only 0.16 to 0.24 will be absorbed, the efficiency of such detectors would be too small for most applications. To overcome this limitation, we designed a detector with a grating that exhibits resonances for both polarizations of the same wavelength.

The simplest way to construct a polarization-independent grating is to introduce corrugations perpendicular to the first grating. Such a 2D grating structure is shown in Fig. 4. A corrugation of the width a_2 and length b_1 leads to a 2D grating. Because the corrugated poly-Si gate also masks the n- and p-well doping, the corrugated gates must not touch each other in the y-direction. The corrugation width a_2 should always be smaller than the grating period a, because otherwise the n- and p-wells will not be connected to each other in the x-direction, and then each well would have to be connected separately with metal contacts. The metal lines needed to contact all these wells would severely disturb the grating, block light from entering the silicon and absorb it before it can reach the Si. By letting the corrugations not touch in the y-direction, contacts can be spaced as far as ~10 μm apart in the x-direction.

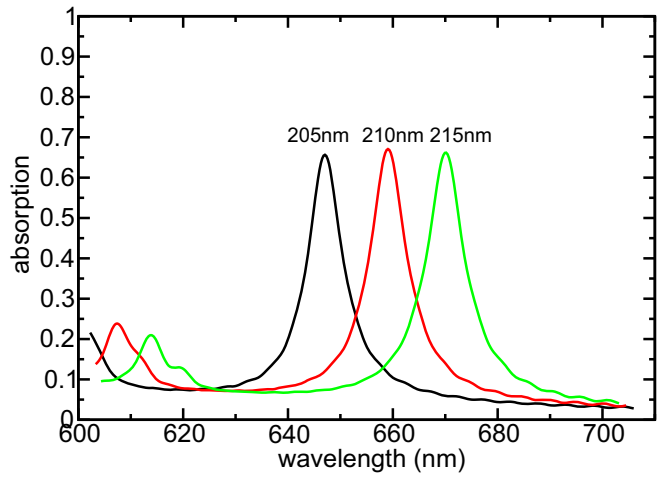


Fig. 5. The calculated absorption spectra of the incident light of the 2D grating as a function of the wavelength for three different grating periods a. The gate width a_1 is 50 nm, the corrugation period b is 210 nm, the corrugation width a_2 is 150 nm, and the corrugation length b_1 is 75 nm. These parameters are kept fixed.

The absorption of these 2D gratings was computed in the same way as for that of the 1D gratings. In the 2D case, the size of the computational cell was $1a \times 1b \times 7a$. For the absorption spectra shown in Fig. 5, the gate width a_1 was fixed to 50 nm, the corrugation period b to 210 nm, the corrugation width a_2 to 150 nm, and the corrugation length b_1 to 75 nm. We vary the grating period a between 205 and 215nm. The absorption peaks of the s- and p-polarization coincide and form one peak exhibiting a maximum absorption of approximately 0.67. Considering that only half the light is absorbed in the depletion region, approximately 0.33 of the light forms electron-hole pairs which then lead to a signal. Therefore, we expect the efficiency of the photo-detectors to be below this value.

III. Fabrication and Measurements

The 1D and 2D photo-detectors designed are fabricated in a standard 45-nm SOI CMOS process. This process features a 1.16-nm-thick gate oxide, advanced activation annealing, and an advanced immersion lithography which provides a good channel length control and supports multiple gate pitches. Four different sizes of photo-detectors, i.e., 75×75, 50×50, 25×25, and 15×15 μm^2 were implemented. A picture of a complete fabricated device is shown in Fig. 6.

The photo-detectors fabricated were characterized as follows. They were excited with 80-fs-wide pulses at a repetition rate of 80 MHz at wavelengths between 620 and 700 nm. The light source was an optical parametric oscillator (OPO), which was pumped by a mode-locked Ti:sapphire laser. The light was attenuated and then coupled into a polarization-maintaining fiber with a mode field diameter of about 5 μm. The latter was positioned within a few microns above the detector surface at variable angles. A wafer probe setup allowed high-speed 50-Ohm opto-electronic measurements over the entire 300-mm wafer. RF (radio-frequency) connections were made through broadband (DC-50 GHz) ground-signal-ground probes from GGB Industries.

Figure 7(a) shows the responsivity of the photo-detector as a function of the wavelength. The parameters used were a = 215 nm, b = 210 nm, a_1 = 75 nm, a_2 = 150 nm, and b_1 = 65 nm. For comparison the computed absorption spectrum is shown in Fig. 7(b). The maximum measured responsivity of

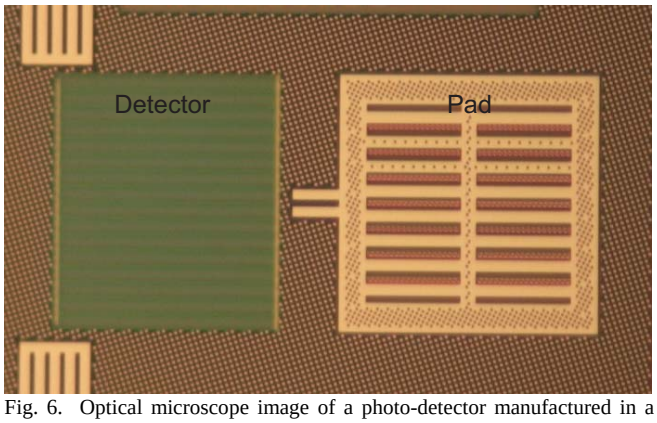


Fig. 6. Optical microscope image of a photo-detector manufactured in a standard SOI CMOS process.

0.016 A/W is observed at a wavelength of 670 nm, which agrees very well with the computed absorption maximum at 674 nm. The much broader peak from the experiment indicates that the two polarization peaks of the real device do not completely coincide. They are shifted in wavelength with respect to each other because of manufacturing tolerances. The edges of the poly-Si gates and the SiN_3 capping are likely rounded, and the gates do not have exact design dimensions because of fabrication inaccuracies. In Fig. 7, two additional experimental peaks at 632 and 645 nm can be observed. These peaks are attributed to the computed absorption peak at 620 nm.

The responsivity of the photo-detector with a 2D grating was compared with that of one with a 1D grating. We measured the 1D photo-detector in the same way, which yields a maximum responsivity of 0.0049 A/W, approximately 3.3 times smaller than that of the 2D device. This is in excellent agreement with the computed absorption of the 1D photo-detector, which is 2.8 to 4.2 times smaller than that of the 2D photo-detector.

For the photo-detectors with the largest responsivity, we measured a maximum value of 0.04 A/W. This is lower than expected and should be beyond 0.1 A/W for practical applications. To examine this low responsivity, we reviewed the fabrication steps. The metal contacts and poly gates are coated with nickel and platinum to form silicides, which improves their conductivity. In our configuration all *n*+, *p*+ and poly surfaces were heavily covered by silicide. These silicides exhibit a high metal content. Computations confirm that in these areas a large fraction of the light is being absorbed. When including the silicides in the computer model, almost all the light is absorbed by them and only 1% reaches the depletion region. This agrees very well with the small responsivity of 0.0049 A/W we measured. For future devices, it is a good advice to minimize the deposited nickel and platinum in the grating areas. All areas except contacts should be blocked from silicide. This however does not require any process modification, and a mask for this purpose already exists in the design flow.

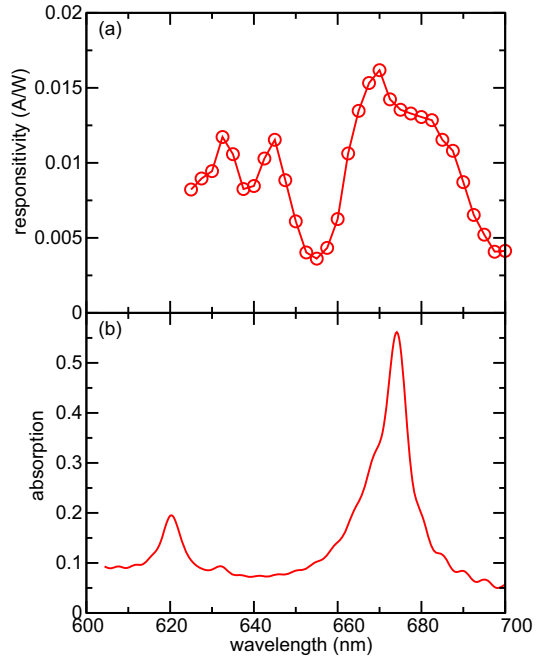


Fig. 7. (a) The measured responsivity as a function of the wavelength for the photo-detector with the parameters a = 215 nm, b = 210 nm, a_1 = 75 nm, a_2 = 150 nm, and b_1 = 65 nm. (b) The calculated absorption spectrum of the grating as function of the wavelength for the same device.

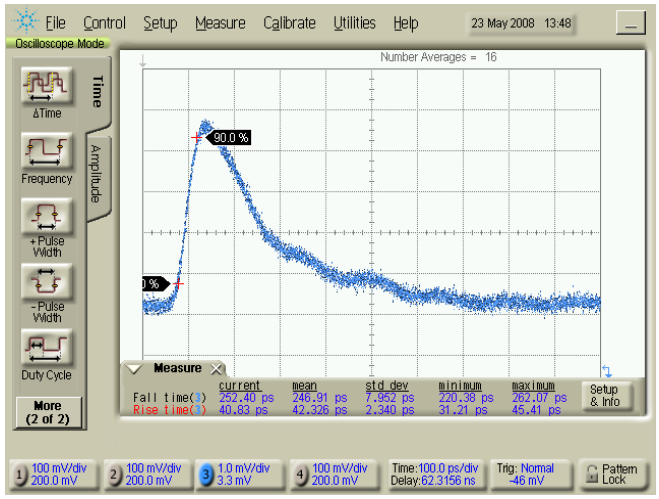


Fig. 8. Time domain measurements for the same photo-detector device as in Fig. 7.

Figure 8 shows the electrical time-domain response of the photo-diode shown in Fig. 7 measured with a 50-GHz sampling oscilloscope. A fast rise time of 42 ps is measured. The relatively slow fall time is attributed to the carriers generated in the *p*+ and *n*+ regions which are removed by diffusion. For data communication applications, slow fall times are not that critical because they can be compensated by means of DFEs (Decision Feedback Equalizer).

IV. Summary and Conclusion

We demonstrated a polarization independent photo-detector device with enhanced responsivity, which is fully compatible with standard SOI CMOS technology. The measured average responsivity is between 0.01 to 0.02 A/W, and a maximum responsivity of 0.04 A/W was demonstrated. The responsivity depends on the wavelength and matches the computed absorption spectra reasonably well. Because of manufacturing tolerances, the peaks are slightly shifted and broadened. The larger deviation of the computed and measured responsivity is due to deposited nickel and platinum, which form silicides. For future diode structures, silicide blockage can avoid this problem.

References

[1] H. Zimmermann, Integrated Silicon Optoelectronics, Berlin: Springer, 2000.

[2] S. Assefa, F. Xia, S.W. Bedell, Y. Zhang, T. Topuria, P. M. Rice, and Y. A. Vlasov, "CMOS-Integrated 40 GHz germanium waveguide photodetector for on-chip optical interconnects," Optical Fiber Communication Conference (OFC), OMR4 (2009).

[3] Weiquan Zhang and Mansun Chan, "Properties and Design Optimization of Photo-Diodes Available in a Current CMOS Technology," Proceedings 1998 Electron Devices Meeting, Hong Kong, 1998, pp. 22-25.

[4] Min Yang, Kern Rim, D. Rogers, J. Schaub, J. Welser, D. Kuchta, D. Boyd, F. Rodier, P. Rabidoux, J. Marsh, A. Ticknor, Qingyun Yang, A. Upham, and S. Ramac, "A High-speed, High-sensitivity Silicon Lateral Trench Photodetector ," IEEE Electron Device Letters, vol. 23, 2002, pp. 395-397.

[5] C. Schow, L. Schares, S. Koester, G. Dehlinger, R. John, and F. Doany, "A 15-Gb/s 2.4-V Optical Receiver Using a Ge-on-SOI Photodiode and a CMOS IC," IEEE Photonics Technology Letters, vol. 18, 2006, pp. 1981-1983.

[6] D. Mathine, "The Integration of III-V Optoelectronics with Silicon Circuitry," Selected Topics in IEEE Journal of Quantum Electronics, vol. 3, 1997, pp. 952-959.

[7] S. Csutak, S. Dakshina-Murthy, and J. Campbell, “CMOS-Compatible Planar Silicon Waveguide-Grating-Coupler Photodetectors Fabricated on Silicon-on-Insulator (SOI) substrates,” IEEE Journal of Quantum Electronics, vol. 38, 2002, pp. 477-480.

[8] A. Farjadpour, D. Roundy, A. Rodriguez, M. Ibanescu, P. Bermel, J.D. Joannopoulos, S.G. Johnson, and G.W. Burr, “Improving Accuracy by Subpixel Smoothing in the Finite-Difference Time Domain,” Optics Letters, vol. 31, Oct. 2006, pp. 2972-2974.